Amendments to the Specification:

Please replace the paragraph beginning on page 6, line 24, with the following rewritten paragraph:

As shown in Fig. 2, the voltage regulating circuit 110 includes a voltage comparator 111, a resistor 112, a capacitor 113, a saw tooth wave superposing circuit 114 and an OR circuit 115. The resistor 112 and the capacitor 113 ~~forms~~ form a low-pass filter, which ~~smooth~~ smooths a portion of the output voltage of the vehicle generator divided by the resistors 172, 174. The smoothed voltage is inputted to a negative terminal of the voltage comparator 111. The saw tooth wave superposing circuit 114 superposes a saw tooth signal of a prescribed cycle (e.g. 5 ms) on the regulation voltage Vreg (correctly, a portion of the regulation voltage Vreg divided by the resistors 172, 174) provided by the signal transmission control circuit 140 and provides reference voltage V1, which is inputted to a positive terminal of the voltage comparator 111. The voltage comparator 111 compares the smoothed voltage that corresponds to the generator's output voltage with the reference voltage V1 that is inputted from the saw tooth wave superposing circuit 114. If the smoothed voltage is lower than the reference voltage V1, the voltage comparator 111 provides a high level signal. On the other hand, it provides a low level signal if the smoothed voltage is higher than the reference voltage V1. The OR circuit 115 provides an output signal that corresponds to a logical sum of the output signal of the voltage comparator 111 and a minimum duty ratio signal. The minimum duty ratio signal has the same cycle as the saw tooth wave signal superposed by the saw tooth wave superposing circuit 114 and also has a minimum duty ratio of about 3 %.

Please replace the paragraph beginning on page 7, line 20, with the following rewritten paragraph:

As shown in Fig. 3, the reference voltage V1 has a wave shape formed by the saw tooth wave superposing circuit 114, and the minimum duty ratio signal has 3%-duty ratio, which is inputted to the OR circuit 115. Thus, the reference voltage having the peak voltage of Vreg and the minimum voltage ~~ofVmin~~ of Vmin each cycle can be provided by superposing the saw tooth wave on the regulation voltage Vreg.

Please replace the paragraph beginning on page 7, line 26, with the following rewritten paragraph:

As shown in Fig. 4, if the output voltage of the vehicle generator 2 is lower than the minimum voltage Vmin, the voltage comparator 111 of the voltage regulating circuit 110 always provides a high level signal. Therefore, the duty ratio of the voltage regulation signal that is outputted from the OR circuit 115 becomes 100 %. If the output voltage of the vehicle generator 2 falls between Vmin and the regulation voltage Vreg, the voltage comparator 111 provides a signal having a duty ratio that is determined by the magnitude relation between the two. Such a signal is outputted from the OR circuit 115 as the voltage regulation signal. If the output voltage of the vehicle generator 2 becomes higher than the regulation voltage Vreg, the voltage comparator 11 always provides a low level signal, so that the OR circuit 115 provides the minimum duty ratio signal whose duty ratio is 3 %.

Please replace the paragraph beginning on page 8, line 12, with the following rewritten paragraph:

The field current detecting circuit 120 detects the field current flowing through the field coil 204 based on the potential of the source of the field current driving transistor 160, which is an N-channel MOSFET. The resistor 170 is connected to the source of the field current driving transistor 160 as a field current detecting resistor. The amount of field current

is detected by the field current detecting circuit 120 based on the voltage difference between opposite ends of the resistor 170 when the field current flows through the source-drain of the field current driving ~~circuit~~ transistor 160 and the resistor 170.

Please replace the paragraph beginning on page 8, line 21, with the following rewritten paragraph:

As shown in Fig. 5, the field current detecting circuit 120 includes an operational amplifier 121, resistors 122, 123 and an A-D converter 124. A prescribed amplifying ratio of the operational amplifier ~~120~~ 121 is determined by the resistors 122, 123, so that an input signal whose voltage is proportional to the amount of the field current is amplified. The A-D converter 124 has an input terminal (IN) to which the amplified signal is inputted and a clock terminal (CL) to which a clock signal CLK of a predetermined frequency is inputted. When the clock signal CLK changes from a high level to a low level, the A-D converter 124 takes in the output voltage of the amplifier 121 to convert it to a digital data (relative to the field current) of a predetermined number of bits. The frequency of the clock signal CLK is n (e.g. 64) times as many as the frequency of the minimum duty ratio signal. The frequency of the clock signal CLK corresponds to the limit of resolution (the number of steps) of the PWM signal.

Please replace the paragraph beginning on page 9, line 9, with the following rewritten paragraph:

The field current control circuit 130 calculates the ~~averagevalue~~ average value of the field current based on the amount of the field current flowing through the field current driving transistor 160. The transmission control circuit 140 controls the field current so that the amount can be less than a field current limit ~~valueIFref~~ value IFref.

Please replace the paragraph beginning on page 10, line 3, with the following rewritten paragraph:

When the key switch is turned on, the ECU 5 starts sending the operation start signal to the transmission terminal X of the generator control system 1. When the transmission control circuit 140 receives the operation start signal via the transmission ~~terminal Z~~ terminal X, it inputs a turn on signal to the terminal S of the power source circuit 100. Thereafter, the power source circuit 100 supplies electric power to various circuits of the vehicle generator control system 1, so that the vehicle generator control system 1 fully operates.

Please replace the paragraph beginning on page 10, line 11, with the following rewritten paragraph:

Thereafter, although the regulation voltage signal and the field current limit signal are sent from the ECU 5, the output voltage of the vehicle generator 2 is controlled to be the regulation voltage Vreg. However, the amount of the field current is so small that the field current control is not carried out. The field current driving transistor 160 is controlled to turn on or off according to the voltage regulation signal having 5ms-cycle outputted by the voltage regulating circuit 110.

Please replace the paragraph beginning on page 10, line 25, with the following rewritten paragraph:

As indicated by a flow diagram shown in Fig. 6, the voltage regulation signal of the voltage regulating circuit 110 is ~~aPWM~~ a PWM signal of 5 milli second cycle. When this signal is inputted to the field current driving transistor 160 via the AND circuit 164, the field current driving transistor 160 turns on and off at 5 milli second intervals at step 100.

Please replace the paragraph beginning on page 11, line 8, with the following rewritten paragraph:

Subsequently, the field current control circuit 130 calculates a control duty ratio of this time Fduty(new) with the following formula (1) based on the last control duty ratio Fduty(old) that is set when the field current driving transistor 160 is turned on last time, the field current limit value IFref and the average value of the field current IFav at step 103. Incidentally, the control duty ratio is a duty ratio of a signal for controlling the field current that is inputted to the AND circuit 164 from the field current control circuit 130. The duty ratio is calculated from an average value of the field current that is detected each time and the signal inputted from the transmission control circuit 140.

$$Fduty\ (new) = Fduty(old) + K(IFref - IFav) \quad \cdots \quad (1)$$

, where K is a positive constant.

Please replace the paragraph beginning on page 11, line 20, with the following rewritten paragraph:

If the average value of the field current IFav is smaller than the field current limit value IFref, the control duty ratio of this time Fduty(new) is replaced by a value that is larger than the control duty ratio of last time Fduty(old). If, on the other hand, the average value of the field current IFav is larger than the field current limit value IFref, the control duty ratio of this time Fduty(new) is replaced by a value that is smaller than the control duty ratio of last ~~timeFduty(old)~~ time Fduty(old).

Please replace the paragraph beginning on page 11, line 27, with the following rewritten paragraph:

The field current control circuit 130 judges whether a current ~~Fduty~~ F duty ratio Fduty(c) is smaller than the control duty ratio of this time Fduty(new) or not at step 104. The

current F duty ratio Fduty(c) is initially set to "1". If the resolution limit of ~~the~~PWM the PWM control is 6 bits, the current F duty ratio Fduty(c) ranges from 1 to 64.

Please replace the paragraph beginning on page 12, line 5, with the following rewritten paragraph:

For example, if the control duty ratio of last ~~time~~Fduty(old) time Fduty(old) is "32" which corresponds to 50% duty ratio, the step 104 provides YES. Thereafter, the field current control circuit 130 adds "1" to the content of the current ~~Fduty~~ F duty ratio Fduty(c) at step 105, takes in the next field current value $IF_{ON(n)}$ at step 106 and ~~calculate~~ calculates an average value of the new field current IFav at step 107 with the following formula (2).

$$IFav = (IF_{ON(l)} + IF_{ON(n)}) /2 \quad \cdots \quad (2)$$

Please replace the paragraph beginning on page 12, line 12, with the following rewritten paragraph:

Thereafter, the operation returns to step 103 and the subsequent steps in which a new control duty ratio of this time is calculated and other processes are repeated. Thus, the current ~~Fduty~~ F duty ratio Fduty(c) gradually increases and the average field current value IFav is calculated each time to renew the current ~~Fduty~~ F duty ratio Fduty(c) until the current duty ratio Fduty(c) becomes larger than the control duty ratio Fduty(new) so that the step 104 provides NO.

Please replace the paragraph beginning on page 12, line 19, with the following rewritten paragraph:

Next, the field current control circuit 130 changes its high level output signal to a low level output signal to change the field current driving transistor from the turn on state to the turn off state at step 108. The field current control circuit 130 holds the ~~current~~Fduty current F duty ratio Fduty(c) as the last control duty ratio Fduty(old) at step 109. The above steps are

carried out in 5ms ~~cycle~~ cycles each time the field current driving transistor 160 switches from its turn off state to its turn on state.

Please replace the paragraph beginning on page 12, line 26, with the following rewritten paragraph:

As shown in Fig. 7, when the field current driving transistor 160 turns on, the field current IF starts increasing. Right after the field current driving transistor 160 turns on, the field current control circuit 130 takes in the initial field current ~~valueIFon(1)~~ value IFon(1) as the average field current value IFav to calculate the control duty ratio of this time Fduty(new) with the formula (1). At this stage, the current ~~Fduty~~ F duty ratio Fduty(c) is "1", which is smaller than the control ~~Fduty~~ F duty ratio of this time Fduty(new), and the field current control circuit 130 takes in the second field current value IFon(2). This kind of operation is repeated until the current ~~Fduty~~ F duty ratio Fduty(c) becomes larger than the control duty ~~ratioFduty(new)~~ ratio Fduty(new), whereby the field current control circuit 130 switches its output signal from a high level signal to a low level signal.